DATA SHEET

SPCP05A

PS/2 3D Mouse Controller

OCT. 17, 2001

Version 1.1

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PS/2 3D MOUSE CONTROLLER

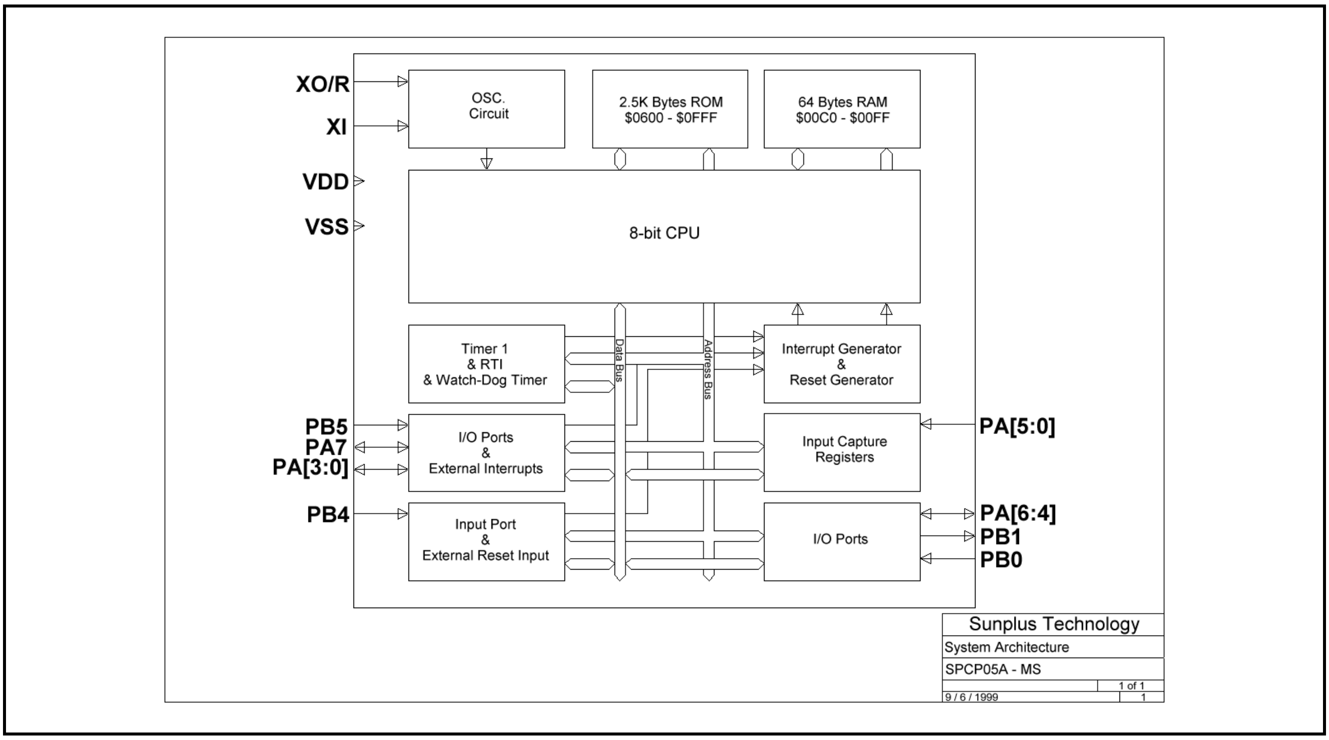
1. GENERAL DESCRIPTION

SPCP05A is a solution on functional improvement from SPMC01. It also includes input capture circuitry for positioning data. It enhances the slew rate control and reduces the output current from 8mA to 4mA on PA port for EMI improvement. In addition, the I/O attribute of PB port is specified for the application. The memory size is similar to SPMC01: 2.5K bytes of ROM and 64 bytes of RAM.

2. FEATURES

- Built-in 8-bit Sunplus CPU core and up to 6.0MHz clock operation.
- Eight general-purpose I/O channels that are grouped as PA port, three pure input channels and one pure output channel are grouped as PB port.
- Three interrupt groups in external.
- External Reset input option on PB4.
- An 8-bit Timer with Real Time Interrupt control.
- A capture circuitry that is combined with one time base and six latches to get counting value.
- A watchdog timer for program control.
- 2.5K bytes of ROM with 64 bytes of RAM.
- R-Oscillation or Crystal input options for system clock.
- Slow Power On Reset respond to the power on slew rate at least 5V/50ms.
- Slew Rate controlled outputs and Balanced Power distribution for EMI improvement.
- Operation voltage 2.5V - 5.5V.

3. BLOCK DIAGRAM



3.1. Functional Block Diagram

3.1.1. CPU

The 8-bit high performance Micro-Controller of SPCP05A is a SUNPLUS processor equipped with the following essential registers: Accumulator, Program Counter, X Register, Stack Pointer and Processor Status Register (The same as 6502 instruction's structure). SPCP05A is a fully static CMOS design. The oscillation frequency could be varied from 100KHz up to 6.0MHz and depends on the application needs. The SPCP05A Development System includes a SUNPLUS ICE, Evaluation Chip and Engineering Development Board.

The content of processor Status Register is:

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Flag	N	V	-	B	-	I	Z	C

N: Negative, V: Overflow, B: Brk command, I: IRQ disable, Z: Zero, C: Carry

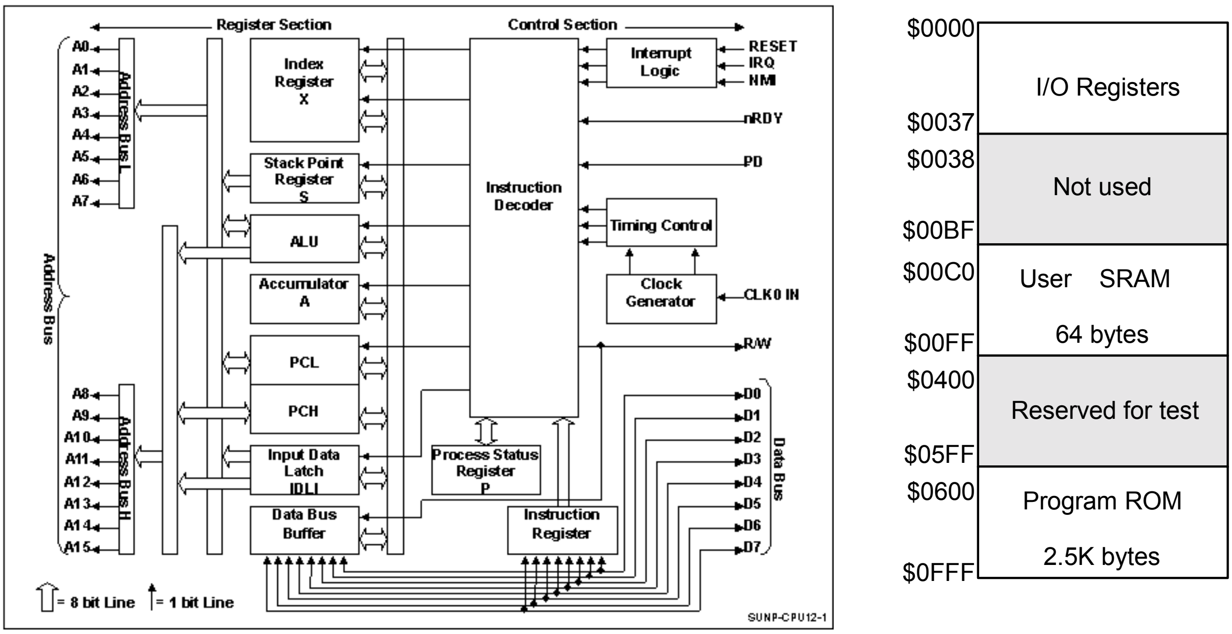


Figure 1. CPU Architecture & Memory Mapping

Sixty-four bytes of RAM (including the stack) are available from $00C0 to $00FF. The stack begins at address $00FF and proceeds down to $00C0. Total of 3072 bytes of ROM on chip includes 2560 bytes of user ROM located from $0600 through $0FFF and 512 bytes of internal test ROM located from $0400 through $05FF. Users' program can only be allocated from $0600 through $0FFF (2.5K).

The address of NMI (not provided in this chip), RESET and IRQ are located from $0FFA to $0FFF. The interrupt vectors should be specified in the program as follows:

```
ORG  $0FFA          ;Define SPCP05A chip interrupt
                     vector.
DW   NMI_ROUTINE
DW   RESET
DW   INT_ROUTINE
```

When using Evaluation board with EPROM (for 27C256), the address of $7FFA must be defined as follows:

```
ORG  $7FFA          ;interrupt vector for EPROM
                     with
DW   NMI_ROUTINE    ;Evaluation Board.
DW   RESET
DW   INT_ROUTINE
```

When using Evaluation board with Sunplus ICE, users fill the **ORG** address of $0FFFA as follows:

```
ORG  $0FFFA         ;interrupt vector for SUNPLUS
                     ICE.
DW   NMI_ROUTINE
DW   RESET
DW   INT_ROUTINE
```

The SPCP05A supports AT-cut parallel resonant oscillated Crystal /Resonator or RC oscillator or external clock sources by mask option (select one out of three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagram listed below is typical X'TAL/ROSC circuits for most applications:

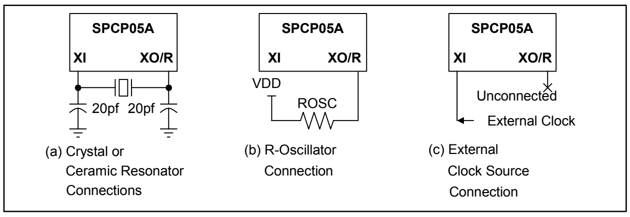


Figure 2. Oscillation Circuit

3.1.2. Register summary

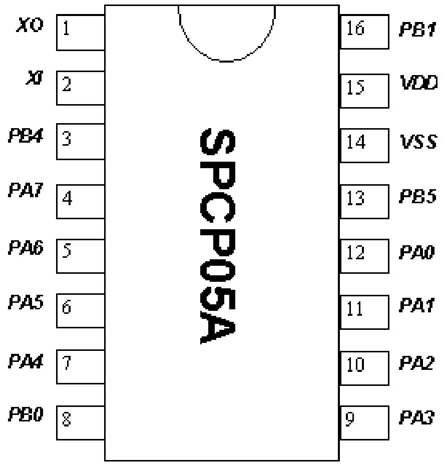
All of the function registers will be set to 0 (except *rt1* and *rt0* in ***TCS1***) when a reset signal occurred. The bits *rt1* and *rt0* will be set to '1' when a reset signal occurred.

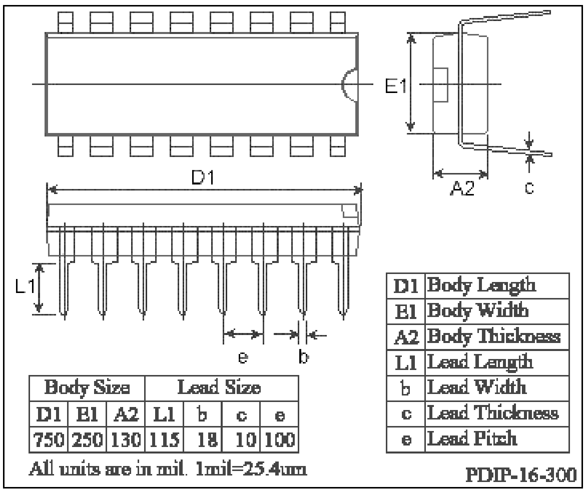
Abbr.	**Register**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Enable**
Addr.	**R/W Control**	**Default Value**								
PA	Port A Data	a7	a6	a5	a4	a3	a2	a1	a0	
$0000	a a a a a a a a	0	0	0	0	0	0	0	0	
PB	Port B Data			b5	b4			b1	b0	
$0001	- - r r - - a r	-	-	0	0	-	-	0	0	
DPA	Port A Data Direction	dpa7	dpa6	dpa5	dpa4	dpa3	dpa2	dpa1	dpa0	0=IN
$0002	w w w w w w w w	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	1=OUT
DPB	Port B Data Direction	sle		dpb5	dpb4			dpb1	dpb0	0=IN
$0003	- - - - - - - -	1	-	0	0	-	-	1	0	1=OUT
TCS1	Timer Ctl. & Status 1	tof1	rtif	tofe1	rtie	tofr1	rtifr	rt1	rt0	
$0004	r r a a w w a a	0	0	0	0	(0)	(0)	1	1	1=SET
TCR1	Timer Counter Reg. 1	tm1r[7:0]								
$0005	r r r r r r r r	0	0	0	0	0	0	0	0	
IRQS	IRQ Control & Status	irqr1	irqr			irqf	irqf1	irqe1	irqe	
$0006	w w - - r r a a	(0)	(0)	-	-	0	0	0	0	
CPWD	CMP & WDT Status								wdt	
$0007	- - - - - - - w	-	-	-	-	-	-	-	0	1=CLR
RPA	Port A Pull-up/down			rpa5	rpa4	rpa3	rpa2	rpa1	rpa0	
$0009	- - w w w w w w	-	-	(0)	(0)	(0)	(0)	(0)	(0)	
RPB	Port B Pull-up			rpb5	rpb4				rpb0	
$000A	- - w w - - - w	-	-	(0)	(0)	-	-	-	(0)	

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Description
XO	1	*Crystal In Or Resistor In*. An external resistive pull-up is connected with internal OSC circuitry for generating the internal clock in R-Oscillation mode. It will be connected with external crystal for crystal oscillation circuitry in crystal mode.
XI	2	*Crystal Output or External Clock Input*. External clock input is connected with internal clock circuitry to generate the internal clock for crystal oscillation circuitry in crystal mode.
PB4	3	*Port B4 Input*. General-purpose input. It also can be used as the Main nRESET input.
PA[7:6]	4,5	*GPIO Port A Bit [7:6]*. General-purpose inputs/outputs with EMI output control. Use DPA to configure it. In addition, PA7 can be used as the external interrupt inputs.
PA[5:0]	6:7,9:12	*GPIO Port A Bit [5:0]*. General-purpose inputs/outputs with EMI output control. Use DPA to configure it.
PB0	8	*Port B0 Input*. General-purpose input.
PB5	13	*Port B5 Input*. General-purpose input. It also can be used as the external Main IRQ input.
VSS	14	*System Ground*.
VDD	15	*System Power Supply*.
PB1	16	*Port B1 Output*. General-purpose output with EMI output control.

4.1. PIN Assignment & Package Outline





4.2. Port A Registers & PINs

There are data register, direction control register, and pull up-down control register built in for PortA access and control. The port A pins are controlled by these registers. Data register (PA) is a read/write accessible register. The Direction Control Register (DPA) and the Pull Up-Down Register (RPA) just can be written and read as "0". All of the output pins are slew rate controlled cell for EMI improvement. The detail description is shown below:

PA	Port A Data Register				$0000
Name	**Bit**	**RW**	**Dft**	**Functional Description**	
a[7:0]	[7:0]	A	0h	*Port A Data.* When Port A is programmed as output pin, the output data on Port pins are determined by PA data register. When Port A is programmed as input pin, any "read" command on Port A Data Register will reflect the logic status of those I/O pins. PA data register will be set to "0" when RESET occurred.	

DPA	Port A Data Direction Register				$0002
Name	**Bit**	**RW**	**Dft**	**Functional Description**	
dpa[7:0]	[7:0]	W	0h	*Port A Data Direction.* Port A can be programmed as input or outputs by DPA register. When dpan="1", the corresponding pins are programmed as outputs. When dpan="0", the corresponding pins are programmed as inputs. DPA will be set to "0"(input) when RESET occurred.	

RPA	Port A Pull Up-Down Register				$0009
Name	**Bit**	**RW**	**Dft**	**Functional Description**	
resv.	[7:6]	-		*Reserved.*	
rpa[5:0]	[5:0]	W	0h	*Port A Pull Down Disable.* When the bit is '0', the build in pull down resistor of the corresponding pins at input mode will be enabled. When it is '1', the pull down resistor will be disabled. Pull down resistors is invalid during output mode. RPA will be set to "0"(enable mode) by RESET.	

More information of the port A pins is shown below:

Pins	Pull Up-Down	R Value	In	Out	Source/Sink	Special Function
PA7	Always Pull Up	5KΩ	IS	OD	-/8mA	*Ext. IRQ1.* Refer to **Interrupt** for more detail.
PA6	Always Pull Up	5KΩ	IS	OD	-/8mA	-
PA5	Pull Down @ rpa5	20KΩ	I	O	4/4mA	-
PA4	Pull Down @ rpa4	20KΩ	I	O	4/4mA	-
PA3	Pull Down @ rpa3	20KΩ	I	O	4/4mA	*Ext. IRQ0.* Refer to **Interrupt** for more detail.
PA2	Pull Down @ rpa2	20KΩ	I	O	4/4mA	*Ext. IRQ0.* Refer to **Interrupt** for more detail.
PA1	Pull Down @ rpa1	20KΩ	I	O	4/4mA	*Ext. IRQ0.* Refer to **Interrupt** for more detail.
PA0	Pull Down @ rpa0	20KΩ	I	O	4/4mA	*Ext. IRQ0.* Refer to **Interrupt** for more detail.

Note: Equivalent Pull down resistance on PA[5:0] is measured at $V_{IN} = V_{TH}$.

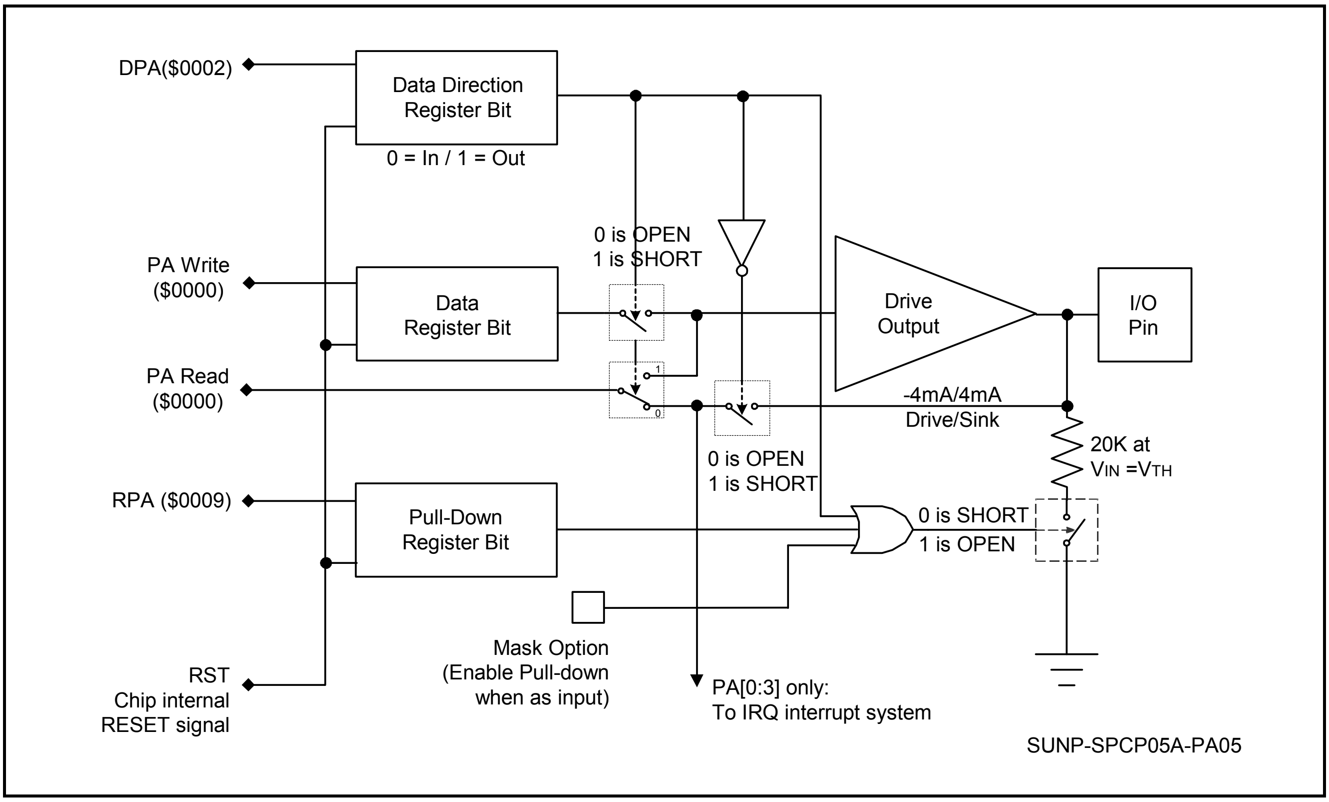


Figure 3. PA[0:5] I/O Diagram

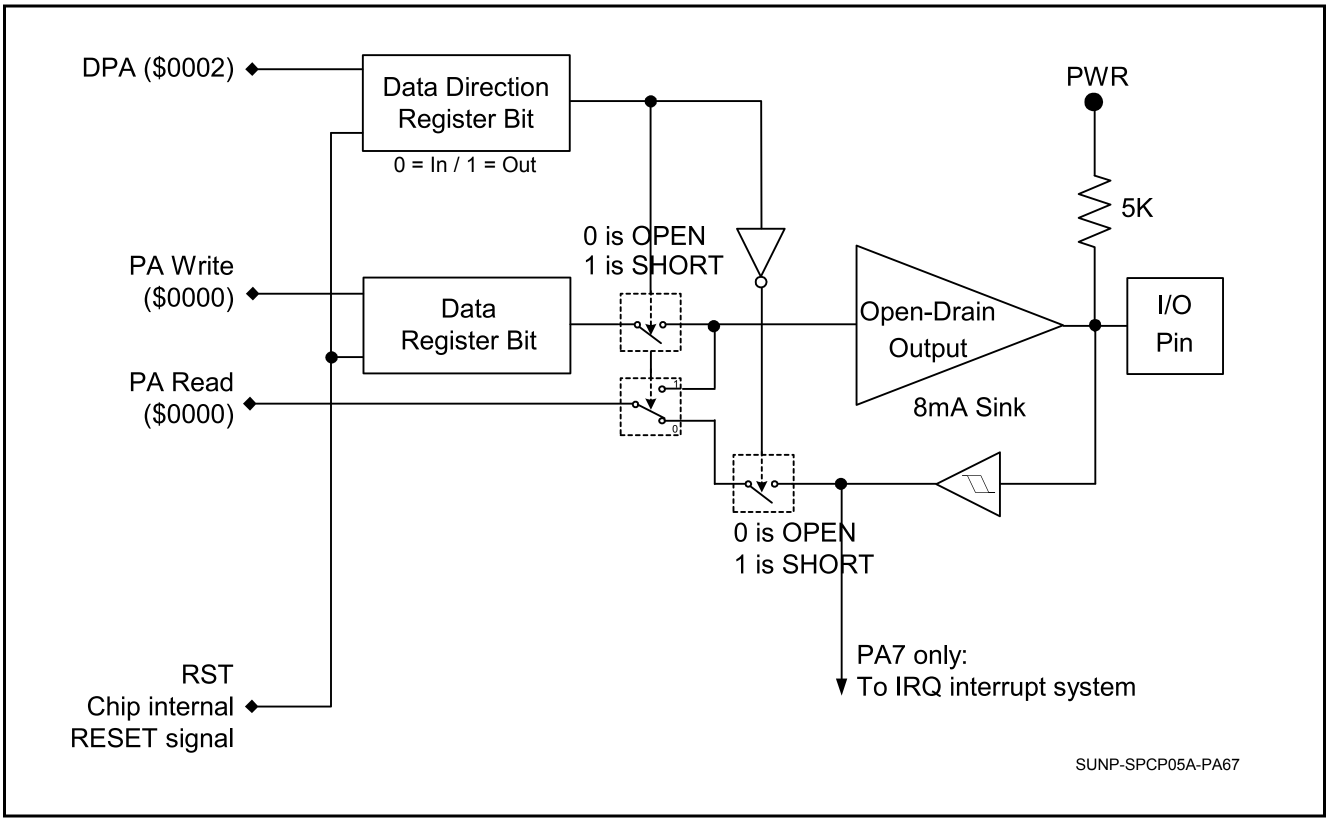


Figure 4. PA[6:7] I/O DIAGRAM

4.3. Port B Registers & PINs

There are data register, direction control register, and pull up-down control register built in for port B accesses and control. The port B pins are controlled by these registers. Data register (PB) is a read/write accessible register. The Direction Control Register (DPB) and the Pull Up-Down Register (RPB) just can be written and read as "0". The output pin, PB1, is slew rate controlled cell for EMI improvement. The detail description is shown below:

PB	Port B Data Register			$0001
Name	**Bit**	**RW**	**Dft**	**Functional Description**
resv.	[7:6], [3:2]	-		Reserved.
b[5:4],b0	[5:4], 0	R	0	*Port B Data on PB[5:4], or PB0.* The pure input pins, PB[5:4] and PB0, reflect the data to these bits. Any "read" command on Port B Data Register will reflect the logic status of those I/O pins. PB data register will be set to "0" when RESET occurred.
b1	1	A	0	*Port B Data on PB1.* PB1 is a pure output pin. The output data on PB1 pin is determined by this bit. PB data register will be set to "0" when RESET occurred.

RPB	Port B Pull Up-Down Register			$000A
Name	**Bit**	**RW**	**Dft**	**Functional Description**
resv.	[7:6], [3:1]	-		*Reserved.*
rpb[5:4], rpb0	[5:4], 0	W	0h	*Port B Pull Up Disable*. When the bit is 0 the build in pull up resistor of the corresponding pins at input mod will be enabled. When it is 1, the pull up resistor will be disabled. Pull up resistors is invalid during output mode. RPB will be set to "0"(enable mode) by RESET.

More information of the port B pins is shown below:

PINs	Pull Up-Down	R Value	In	Out	Source/Sink	Special Function
PB5	Pull Up @ rpb5	10KΩ	IS	-		*Ext. IRQ0.* Refer to **Interrupt** for more detail.
PB4	Pull Up @ rpb4	10KΩ	IS	-		*nRESET.* Use as the external reset input with the Schmitt trigger negative logic.
PB1	No			OD	-/20mA	-
PB0	Pull Up @ rpb0	10KΩ	IS	-		-

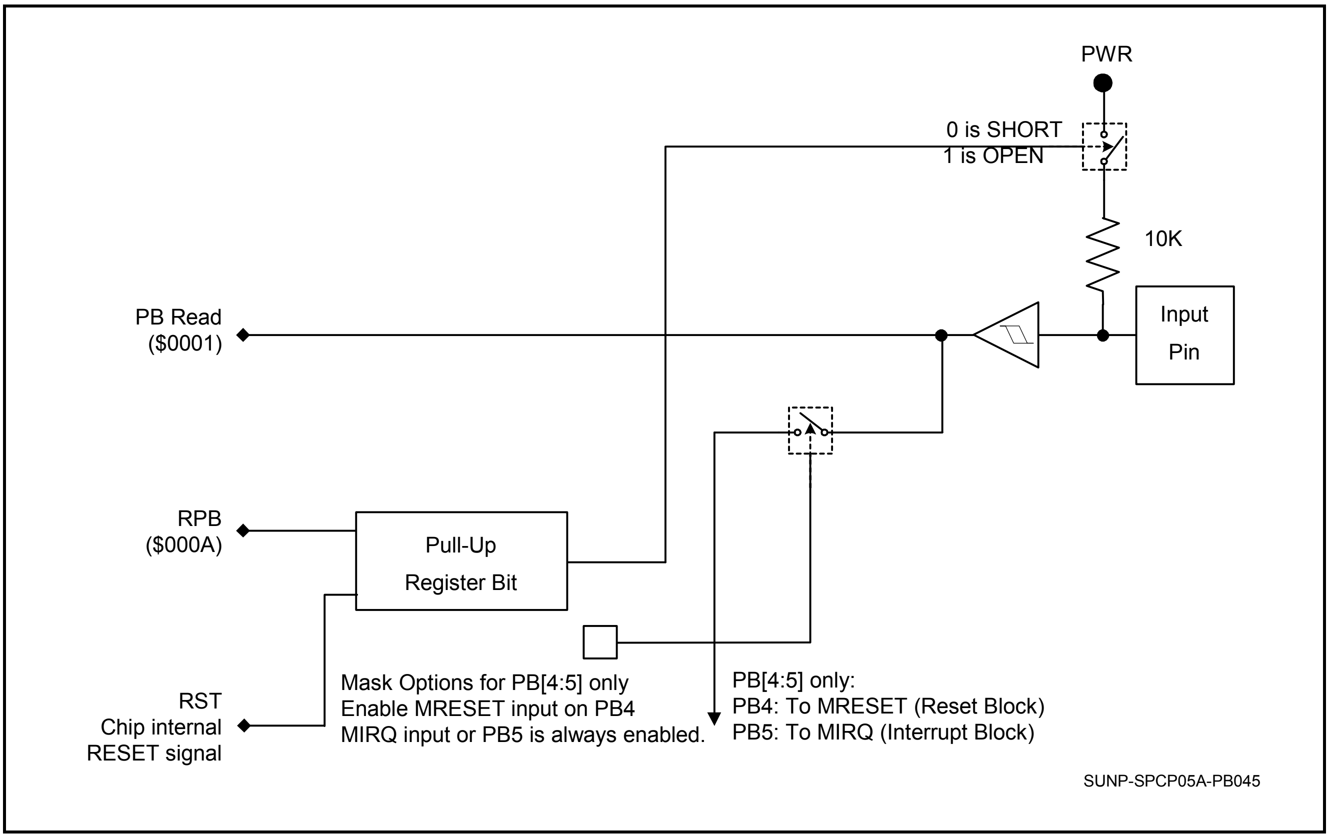


Figure 5. PB[0,4:5] I/O Diagram

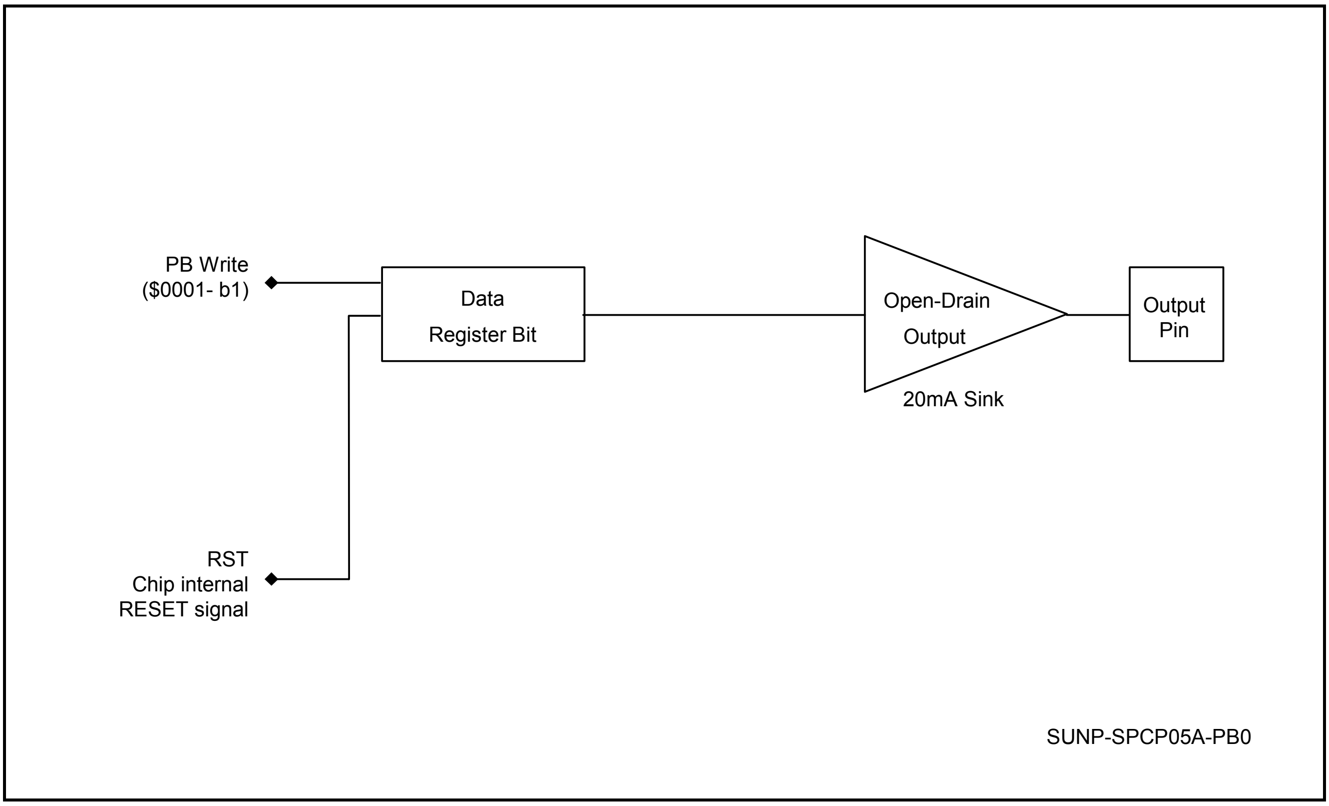


Figure 6. PB1 I/O Diagram

4.4. Interrupt

There are three types of interrupt, Software Interrupt, External Interrupt, and Timer Interrupt. Software interrupt is generated by the instruction BRK. External interrupt is come from IRQ0 and IRQ1. These IRQ signals are combined with the specific function to generate the interrupt. Timer interrupt is generated by the Timer1 that will be described in detail in section ***WDT, Timer1 & Real Time Interrupt***.

The interrupt source diagram is shown in Figure 7-9. The control register for external interrupts is defined in detail as below:

IRQS	IRQ Control & Status Register				$0006
Name	**Bit**	**RW**	**Dft**	**Functional Description**	
irqr1	7	W		*irqf1 Clear bit.* It is used to clear the irqf1 flag. 0: no clear, 1: clear irqf1.	
irqr	6	W		*irqf Clear bit.* It is used to clear the irqf flag. 0: no clear, 1: clear irqf.	
resv.	[5:4]	-		*Reserved.*	
irqf	3	R	0	*Interrupt Flag bit of PB5 or PA[0:3] IRQ0 Input.* It is the flag of interrupt requests coming from PB5 or PA[0:3]. 0: no interrupt, 1: interrupt requested.	
irqf1	2	R	0	*Interrupt Flag bit of PA7 IRQ1 Input.* It is the flag of interrupt requests coming from PA7. 0: no interrupt, 1: interrupt requested.	
irqe1	1	A	0	*Interrupt Control bit of PA7 IRQ1 Input.* It is used to control the interrupt requests coming from PA7. 0: disable, 1: enable.	
irqe	0	A	0	*Interrupt Control bit of PB5 or PA[0:3] IRQ0 Input.* It is used to control the interrupt requests coming from PB5 or PA[0:3]. 0: disable, 1: enable.	

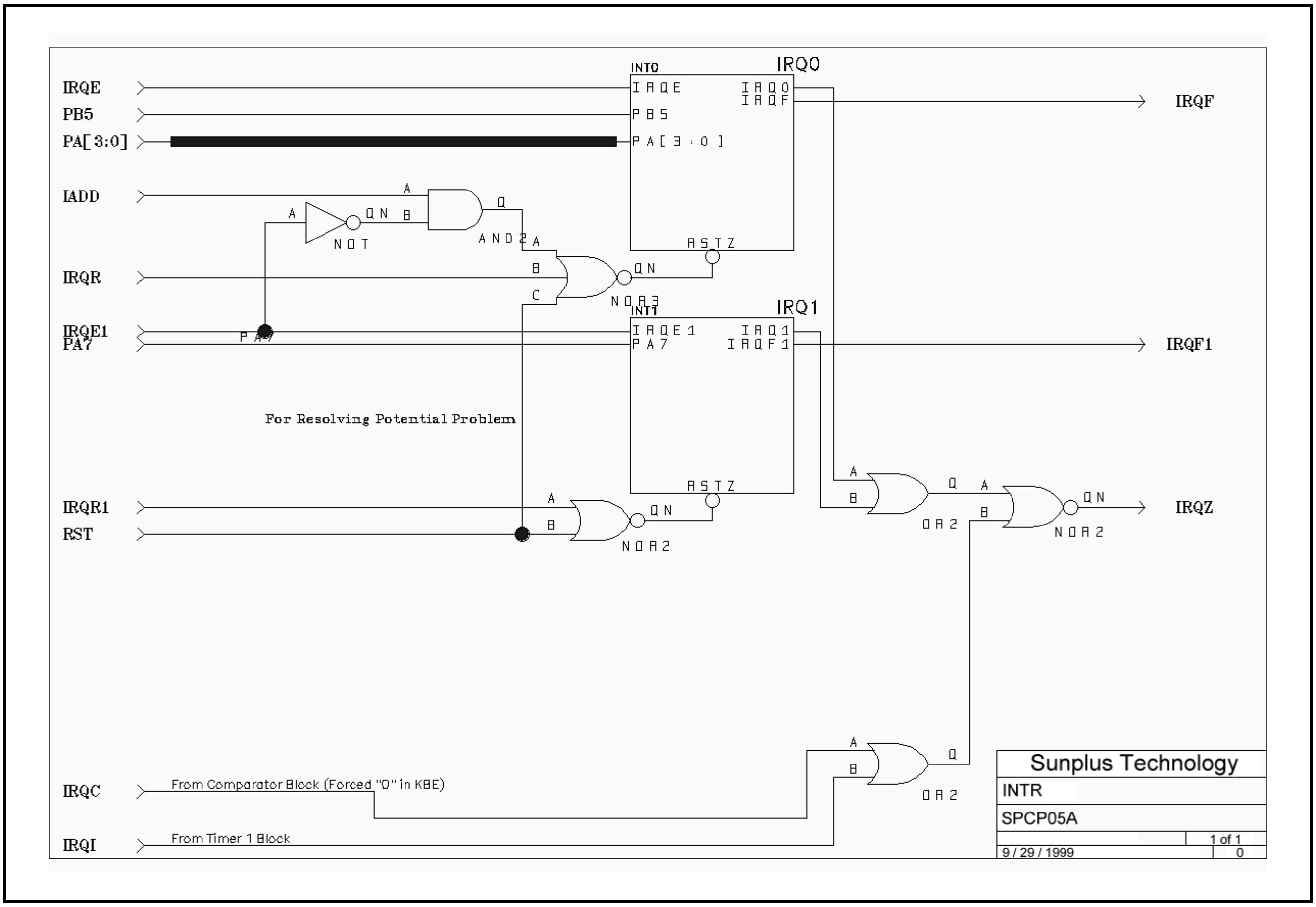


Figure 7. Interrupt Source Diagram

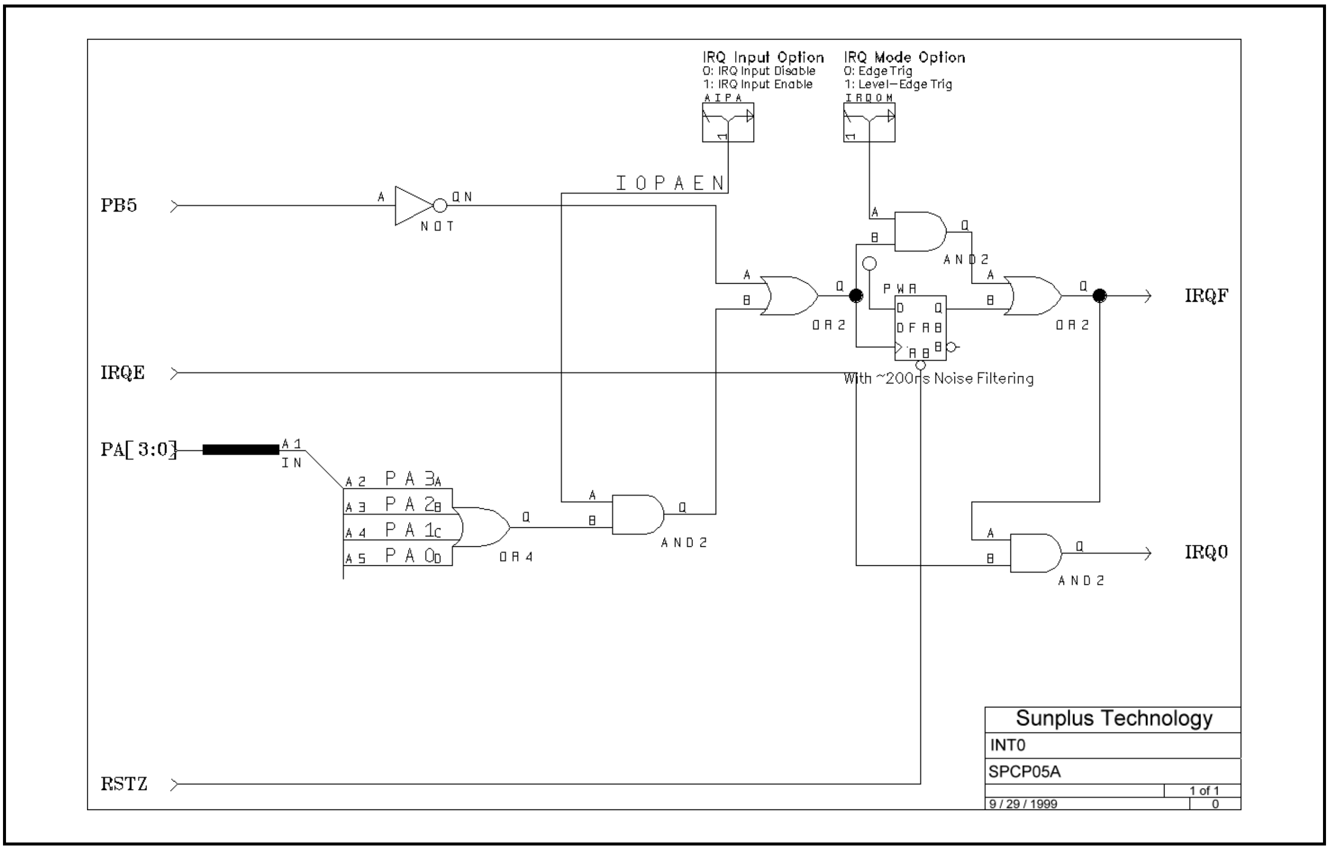


Figure 8. IRQ0 Architecture

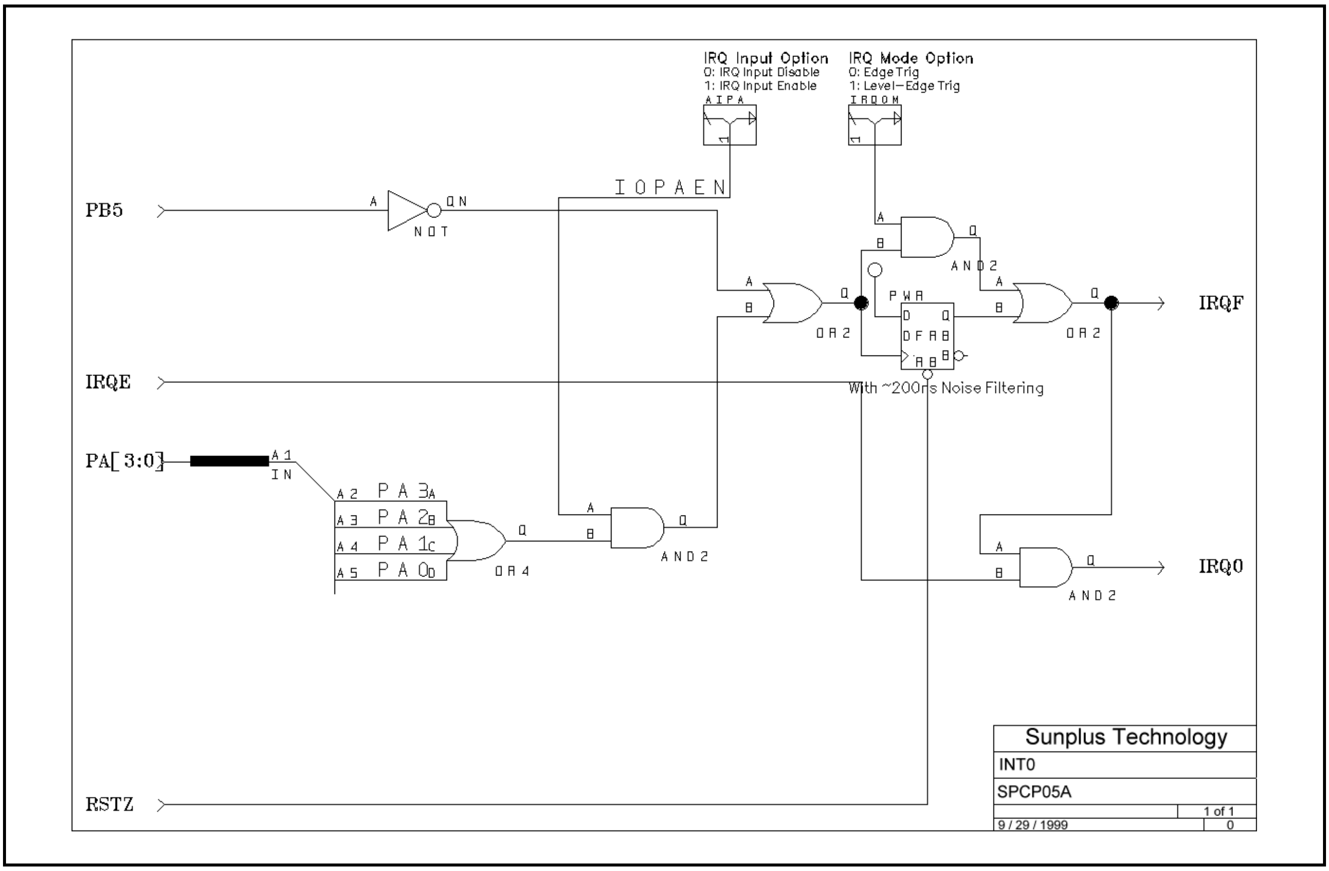


Figure 9. IRQ1 Architecture

4.5. WDT, TIMER1 & Real Time Interrupt

There is an 8-bit timer in Timer 1 with Real Time Interrupt. In addition, a watchdog Timer is built in for the time out reset. It can be enabled or disabled by the mask option. The function of watchdog timer will be described in detail in next section. The related information of Timer is shown below:

TCR1	Timer Counter Register 1				$0005
Name	**Bit**	**RW**	**Dft**	**Functional Description**	
tm1r[7:0]	[7:0]	R	0	*Timer Counter Register 1.* This register is a read-only register. It reports the current value of the beginning 8-bit of timer chain. It is cleared by reset.	

TCS1	Timer Control/Status Register 1				$0004
Name	**Bit**	**RW**	**Dft**	**Functional Description**	
tof1	7	R	0	*Overflow Flag bit of Timer 1*. It is used to indicate the TCR1 rolls over from $FF to $00. 0: no overflow, 1: overflow is set. It can be cleared by writing "1" to tofr1.	
rtif	6	R	0	*Real Time Interrupt Flag bit of Timer 1*. It is used to indicate the status of selected Real Time Interrupt Event of TCR1. 0: no event, 1: event is set. It can be cleared by writing "1" to rtifr.	
tofe1	5	A	0	*Overflow Interrupt Control bit of Timer 1*. It is used to control the interrupt event being generated by tof1 is set. 0: disable, 1: enable.	
rtie	4	A	0	*Real Time Interrupt Control bit of Timer 1*. It is used to control the interrupt event of selected Real Time being generated by rtif is set. 0: no event, 1: event is set. It can be cleared by writing "1" to. 0: disable, 1: enable.	
tofr1	3	W		*Overflow Interrupt Clear bit of Timer 1*. It is used to clear tof1 by writing "1" to this bit. 0: not cleared, 1: clear.	
rtifr	2	W		*Real Time Interrupt Clear bit of Timer 1*. It is used to clear rtif by writing "1" to this bit. 0: not cleared, 1: clear.	
rt[1:0]	[1:0]	A	00	*Selection of Real Time Interrupt Rate*. It is used to select the Interrupt rate for Timer 1. The related rate is shown below.	

CPWD	Comparator & WDT Status				$0007
Name	**Bit**	**RW**	**Dft**	**Functional Description**	
resv.	[7:1]	-		*Reserved.*	
wdt	0	W	0	*Watch Dog Timer Time Out Reset*. It is used to reset Watchdog Timer by writing it as "1".	

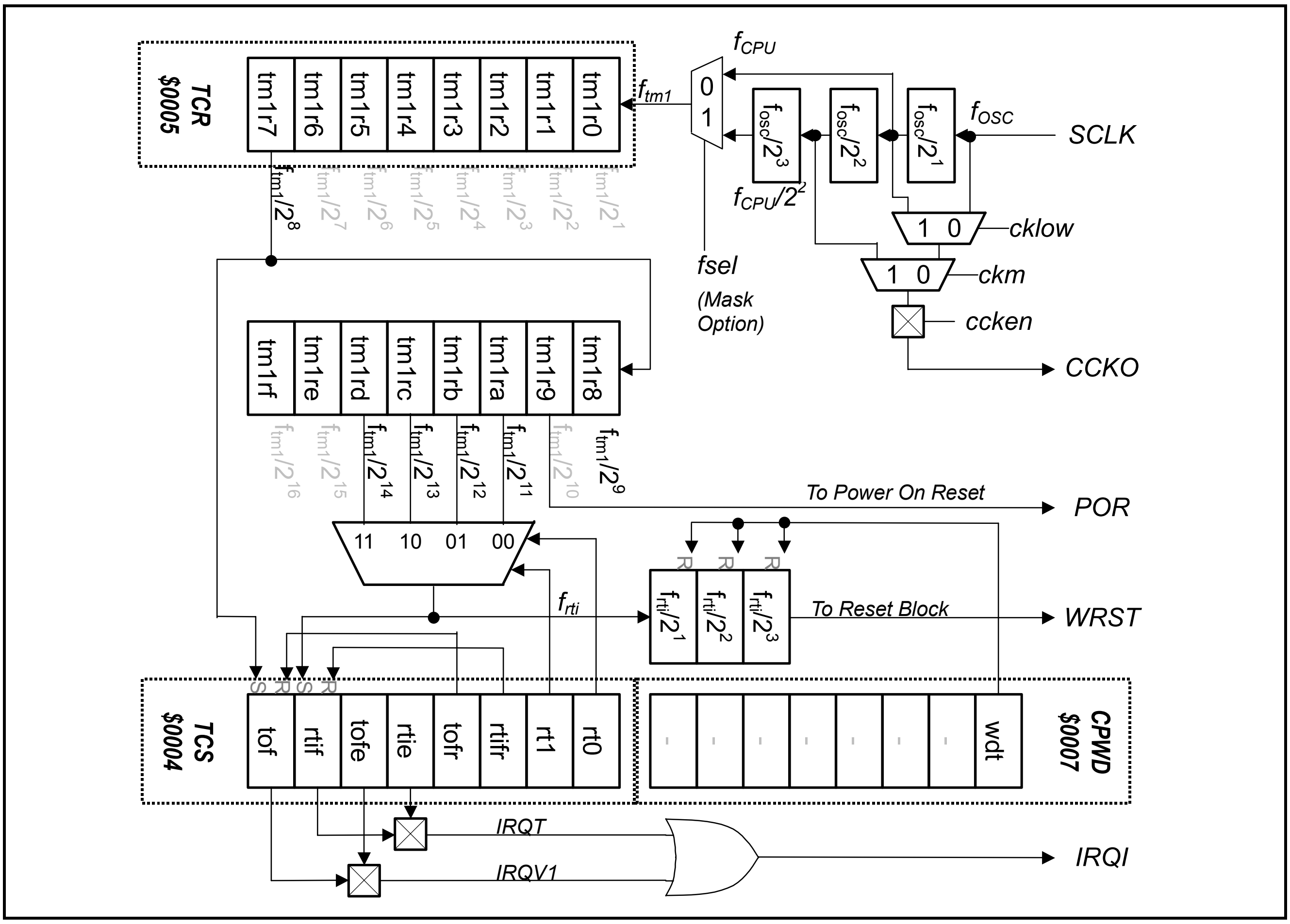


Figure 10. Block Diagram of WDT and Timer 1

4.5.1. RT1: RT0 - Real time interrupt rate select

The RT0 & RT1 control bits select one of four types to let the Real Time Interrupt circuit run. The following table shows an example on interrupt period and WDT reset period on different options for Timer 1 clock input.

Example: CPU Clock f_{CPU} = 1.0MHz (Oscillation Frequency = 2.0MHz) with two options for Timer 1 clock						
RT1:RT0	**RTI RATES**			**MIN. WDT RESET (=RTI/8)**		
	Divider	option $f_{CPU}/4$	option $f_{CPU}/1$	Divider	option $f_{CPU}/4$	option $f_{CPU}/1$
00	2048	8.192ms	2.048ms	16384	65.536ms	16.384ms
01	4096	16.384ms	4.096ms	32768	131ms	32.768ms
10	8192	32.768ms	8.192ms	65536	262ms	66ms
11	16384	65.536ms	16.384ms	131072	524ms	131ms

(RT1, RT0) for RTI & WDT Reset Frequency Table at f_{CPU} = 1.0 MHz

4.6. RESET

There are five types of the reset resources implemented for system reset: Power-On Reset, Low Voltage Reset, Illegal Address Reset, Main External Reset and Watchdog Timer Reset. The last two are optional by mask for customers' configuration. Below shown is the block diagram of Reset.

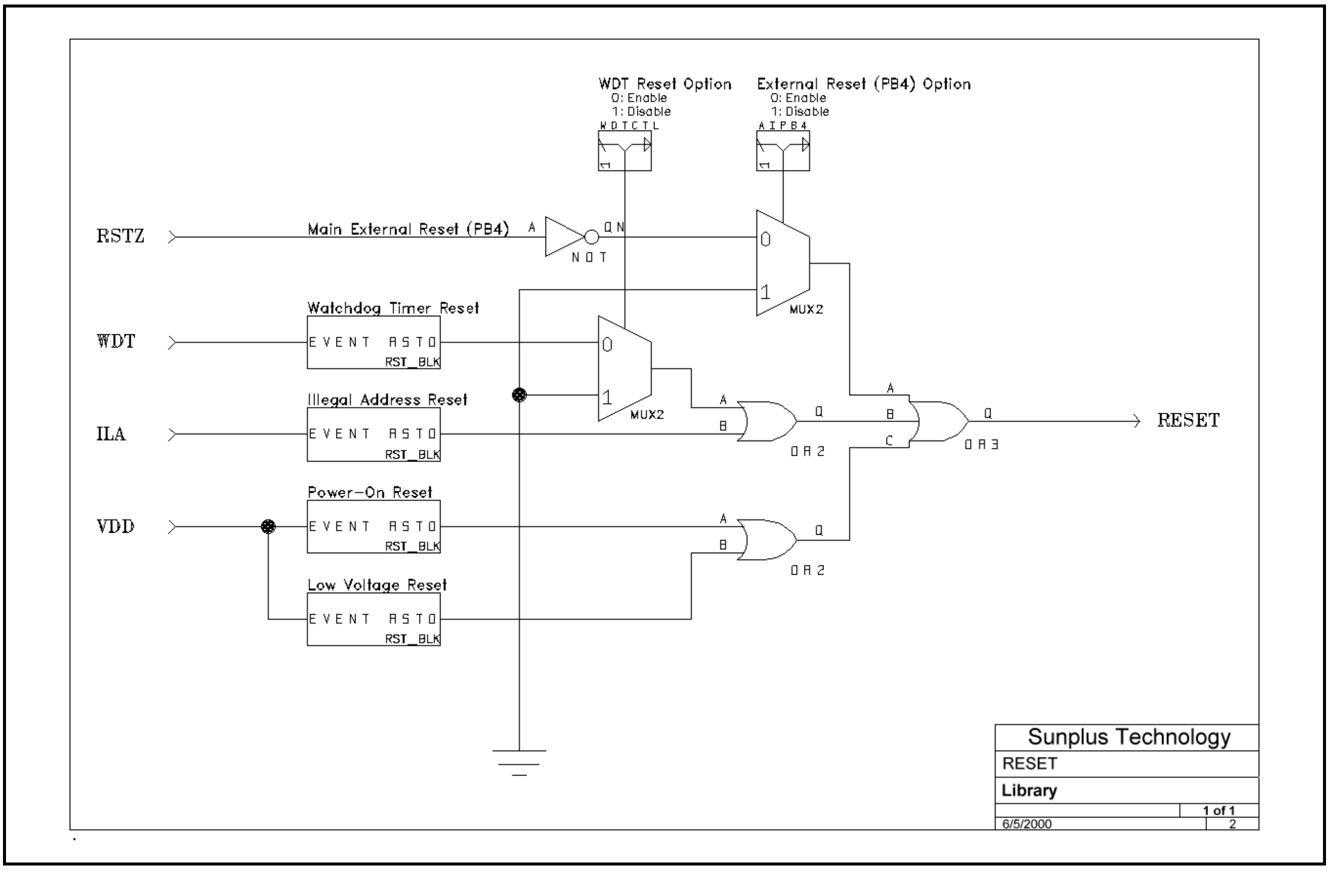


Figure 11. Block Diagram of Reset

Power on Reset is an internal reset. The Power-on-Reset will generate the reset signal that will reset the CPU until oscillator stabilized. The CPU will become active after 50ms in minimum from system reset. To confirm the Power on Reset is generated properly, the system VDD should be held at a zero potential with respect to ground. Improper initial setting of the VDD might cause the Power on Reset to be failed and then the internal can not be initialized properly. In such case, the system is unexpected to work properly.

The Watchdog Timer (WDT) can be disabled or enabled through mask option. The internal reset of WDT will be generated by a time-out of the WDT automatically when watchdog is enabled. It is implemented on this device using the output of the RTI circuit and further dividing it by eight (RT1, RT0 timing times 8). This time out generates reset if the WDT register is not cleared. An internal reset is generated and reset vector fetched. Preventing a WDT time-out reset is done by writing a '1' to WDT ($0007 b0) within a specific time. The min. WDT reset times listed in (RT1, RT0) & WDT Interrupt Frequency Table.

The internal reset of IAR generated when an instruction op-code fetch occurs from an address not implemented in the RAM ($00C0-$00FF) nor ROM ($0400-$0FFF). The IAR will generate the reset signal that will reset the CPU and other peripherals.

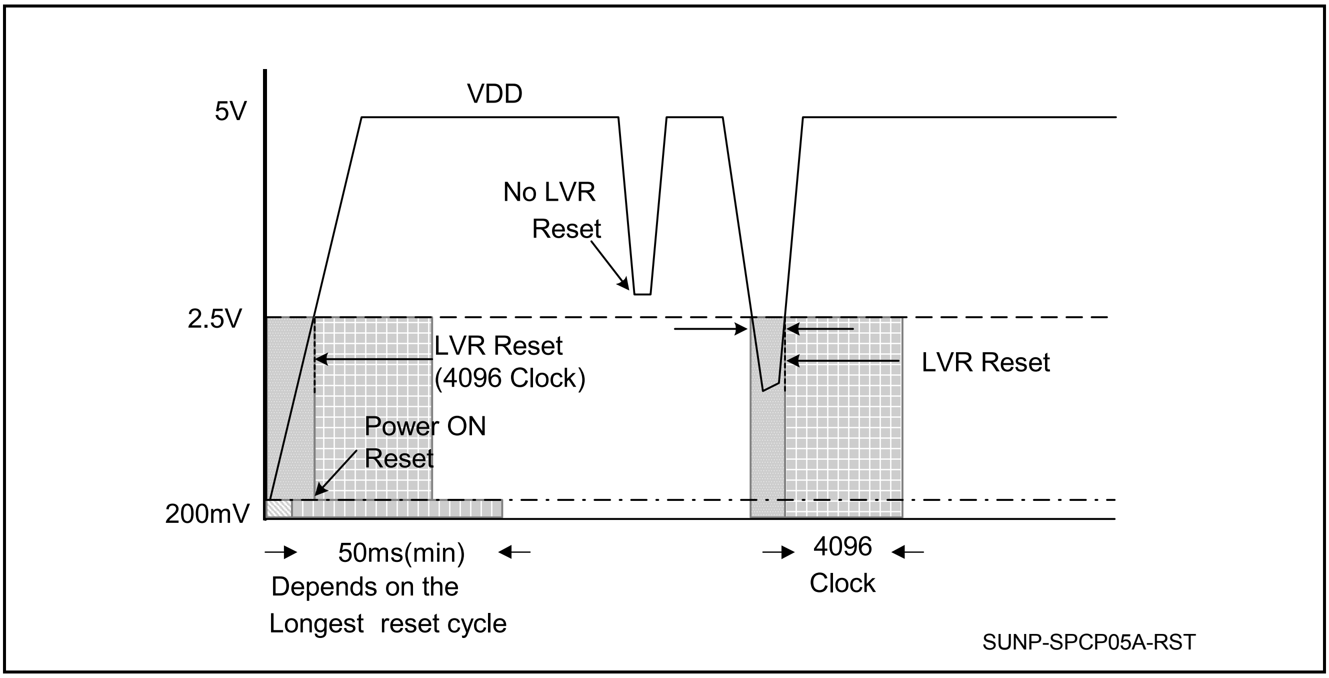


Figure 12. Reset Timing

4.7. Option Table

No.	Name	Relation	Function
1	aipa	PA[3:0] Pin	*Alternative Input Option on PA[3:0] for IRQ0.* 0: Alternative Input is Disabled. 1: Alternative Input is Enabled.
2	aipb4	PB4 Pin	*Alternative Input Option on PB4 for nRESET.* 0: Alternative Input is Enabled. 1: Alternative Input is Disabled.
3	clkext	XI/XO pins	External Clock Input Option. 0: Internal clock mode, depended on OSC mode option, oscm. 1: External clock mode. XO is used to feed in external clock.
4	oscm	XI/XO pins	*Oscillation Mode Option.* 0: Crystal mode, A crystal circuitry is connected to XI and XO for clock generating. 1: R-OSC mode, A Pull up Resistor is placed on XI for internal OSC circuitry to generate the clock.
5	irq0m	IRQ0	*IRQ Trig Mode Option on IRQ0.* 0: Edge Trig. 1: Level-Edge Trig.
6	fsel	Clock	*CPU Clock Divisor Option.* 0: f_{CPU}. 1: f_{CPU} /4.
7	wdtctl	WDT	*Option of Function Control on Watchdog Timer Reset.* 0: Function is enabled. 1: Function is disabled.

5. ELECTRICAL SPECIFICATIONS

5.1. Item Definition

Item	Definition	Item	Definition
V_{IH}	Input High Voltage	I_{OH}	Output High Current (Source)
V_{IL}	Input Low Voltage	I_{OL}	Output Low Current (Sink)
V_{TH}	Input Threshold Voltage	I_Z	Output Leakage Current (Source)
SF_V	Frequency Stability	R_P	Pull-up/down Resistance
DF_V	Frequency Deviation		

5.2. Absolute Maximum Rating

Characteristics	Item	Min.	Typ.	Max.	Unit	Condition
Storage Temperature	T_{STR}	-40	-	70	ºC	
Operating Ambient Temperature	T_{OPR}	0	-	70	ºC	
Voltage Rating on Input	V_{IN}	-0.3	-	VDD +0.3	V	
Voltage Rating on VDD		-0.3	-	7.0	V	
Output Voltage	V_{OUT}	0	-	VDD	V	

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

5.3. Recommended Operating Conditions

Characteristics	Item	Min.	Typ.	Max.	Unit	Condition
Operating Supply Voltage	VDD	2.4	-	5.5	V	
CPU Clock (Internal CPU clock)	f_{CPU}	200K	-	6.0M	Hz	VDD = 5.0V
Power Consumption	I_{DD}	-	3.7	-	mA	f_{CPU} = 6.0MHz @ VDD = 5.0V
Power Up Initial Voltage	V_{INIT}	-	-	1.5	V	
LVR Trigger Voltage	V_{LVR}	2.4	-	-	V	

5.4. PIN Attribute Description (VDD = 5.0V, Temperature = 25ºC)

Mnemonic	Description	Item	Min.	Typ.	Max.	Unit	Condition
PA[5:0]	Input TTL level with Pull Down R option 4mA Output with Slew Rate Control.	V_{IH}	2.0	-	-	V	
		V_{IL}	-	-	0.8	V	
		V_{TH}	1.3	-	2.0	V	0℃ to 40℃
		I_{OH}	4.0	-	-	mA	V_{OH} = 2.4V
		I_{OL}	4.0	-	-	mA	V_{OL} = 0.5V
		I_Z	-	-	10	μA	
		R_P	16	20	24	KΩ	V_{IN} = V_{TH}, 0℃ to 40℃
			40	50	60	-	V_{IN} = VDD = 5V
XI, XO	Special Input Cell Pair for RC oscillation.	SF_V	%	-	-	±5	$(f_{5.5V}-f_{4.5V})/f_{5V}$ *
		DF_V	%	-	-	±10	VDD = 5V
		R_P	KΩ	-	45.3	-	f_{5V} = 5.15MHz
PA[7:6]	Input TTL level with Pull Up R, Schmitt-Triger 8mA Open Drain Output with Slew Rate Control.	V_{IH}	V	2.4	-	-	
		V_{IL}	V	-	-	0.8	
		I_{OL}	mA	8.0	-	-	V_{OL} = 0.5V
		R_P	KΩ	4.0	5.0	6.0	V_{IN} = VSS

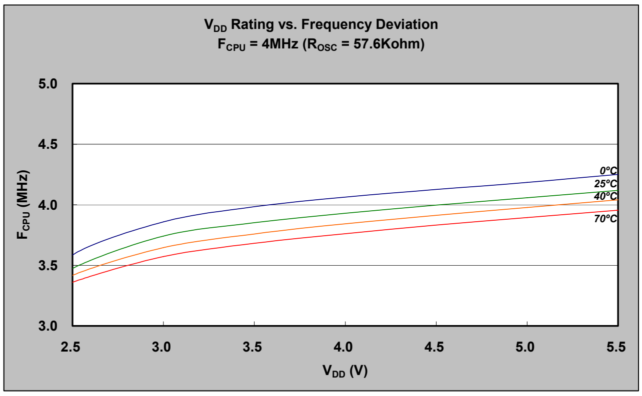
Mnemonic	Description	Item	Min.	Typ.	Max.	Unit	Condition
PB[5:4], PB0	Input CMOS level with Pull Up R, Schmitt-Triger	V_{IH}	V	3.5	-	-	
		V_{IL}	V	-	-	1.2	
		R_P	KΩ	8.0	10	12	V_{IN} = VSS
PB1	20mA Open Drain Output with Slew Rate Control.	I_{OL}	mA	20	-	-	V_{OL} = 0.5V
		I_Z	μA	-	-	10	

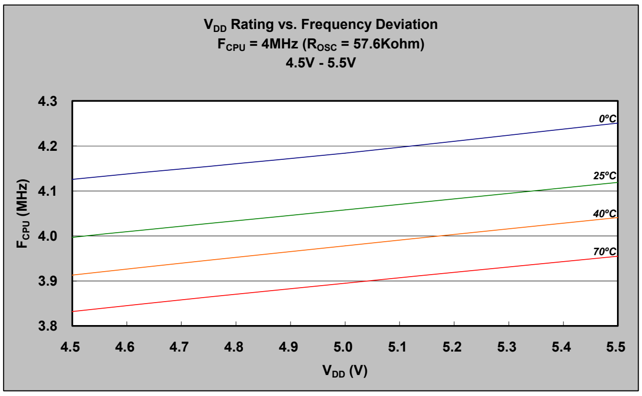
Note: *The frequency defined in this item is based on the CPU frequency. It is one-half of the oscillation frequency.

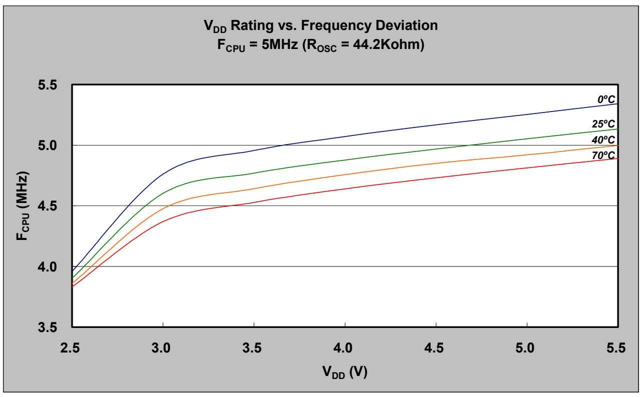
5.5. Timing Diagram (VDD = 4.5V to 5.5V, Temperature = 0ºC to 40ºC or 70ºC)

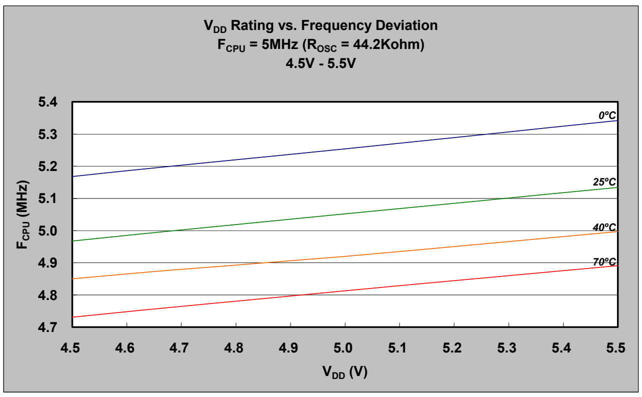
Characteristics	Item	Min.	Typ.	Max.	Unit	Condition
Power On Reset (Ensure POR)	t_{POR}	-	-	120	ms	Option for t_{POR} /2
Output Falling Edge Transition (PA[7:6])	t_R	12 -	15 -	18 20	ns	C_L = 10pf, 90%-10% 40℃/ 70℃
Output Falling Edge Transition (PB1)	t_R	12 -	15 -	18 20	ns	C_L = 10pf, 90%-10% 40℃/ 70℃
Output Rising Edge Transition (PA[5:0])	t_R	17 -	22 -	27 29	ns	C_L = 10pf, 10%-90% 40℃/ 70℃
Output Falling Edge Transition (PA[5:0])	t_F	14 -	17 -	20 22	ns	C_L = 10pf, 90%-10% 40℃/ 70℃

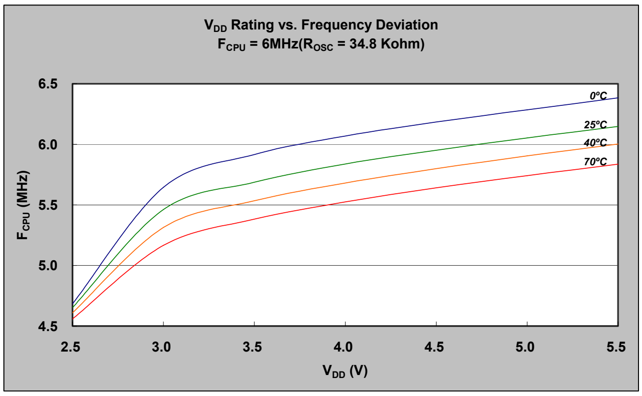
5.6. R-Osc Mode Frequency Curve (Normalized Data)

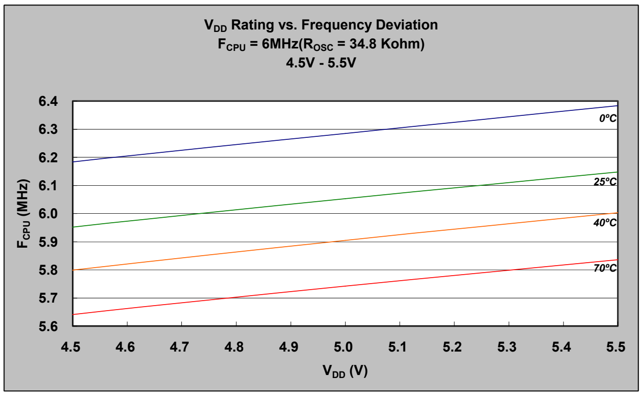




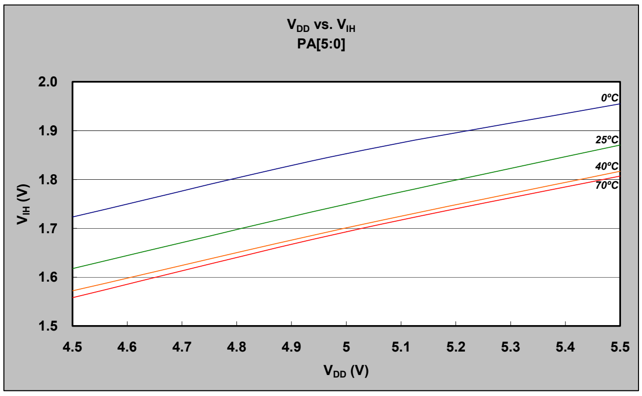


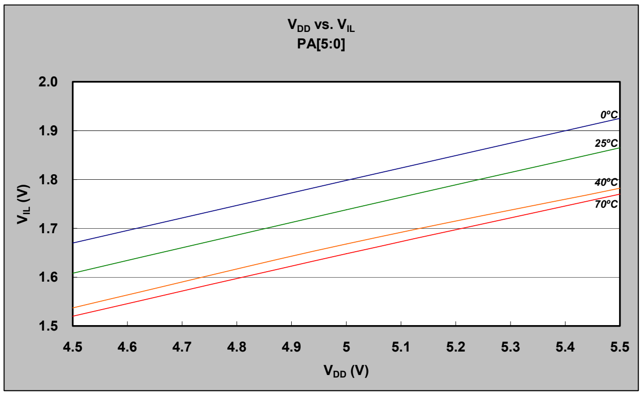




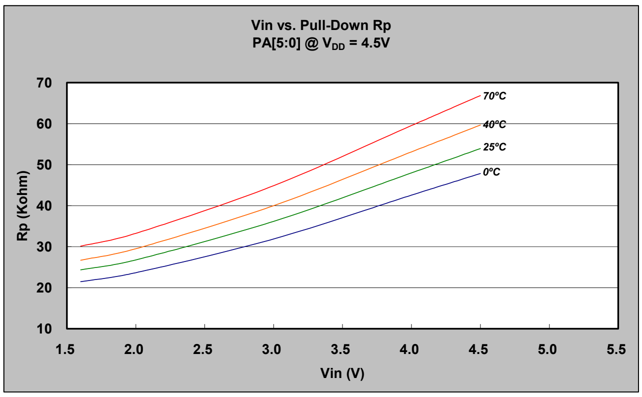


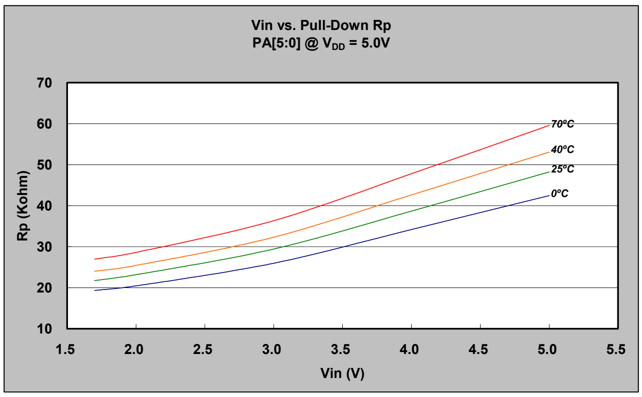
5.7. PA[5:0] V_{IH} and V_{IL} Distribution Curve (Normalized Data)

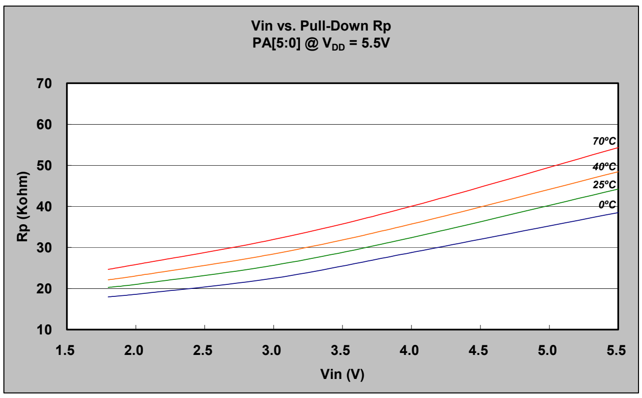




5.8. PA[5:0] Pull Down Resistance Distribution Curve (Normalized Data)







6. DISCLAIMER

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7. REVISION HISTORY

Date	Revision #	Description	Page
SEP. 05, 2001	1.0	Original	
OCT. 17, 2001	1.1	1. Revise Timer1 Block Diagram and I/O attribute on Port B Data Register 2. Renew to a new document format	